REMARKS

Claims 1-7, 9-27, and 29-32 were pending. Claims 40-43 have been added. Accordingly, claims 1-7, 9-27, 29-32, and 40-43 remain pending subsequent entry of the present amendment. New claims 40-43 are supported by at least claim 27 and pages 15-16 of the Description. No new matter has been added.

Specification Amendment and Requested Information

Please find enclosed a copy of Section 5 of the Software User's Manual for the MIPS32 Processor Core Family as requested in paragraph 2 of the Office Action. Also enclosed is Section 6 of the Software User's Manual for the MIPS64 Processor Core Family.

Pursuant to the examiner's request, the specification has been amended to delete the hyperlink reference.

Not All Claims Addressed

Applicant notes that while claims 1-7, 9-27, and 29-32 are currently pending, only claims 10-14, 16-17, 20-24, 27, and 29-30 are addressed in the present Office Action. None of claims 1-7, 9, 15, 18-19, 25-26, 28, or 31-32 are addressed as required. (see, MPEP 707.07; MPEP 707.07(i)). Further, the unaddressed claims are not identical to those addressed. Applicant further notes, for example, the rejection of claim 1 in the prior office action was on a different basis than that of the rejection of claim 10. Accordingly, the Office Action is not complete and Applicant is not able to properly address any objections or rejections the examiner may have regarding these unaddressed claims. Therefore, should the examiner deem it necessary to issue a further office action, Applicant requests the further office action be non-final in order to allow the Applicant an opportunity to properly respond.

35 U.S.C. § 103(a) Rejections

In the present Office Action, claims 10-14, 16-17, 20-24, 27, and 29-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" (hereinafter "MCF5206") and Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" (hereinafter "MCF5206 Addendum"), in view of US Patent No. 5,025,368 (hereinafter "Watanabe"). However, Applicant submits each of the pending claims recite features that are neither disclosed nor suggested in the combination of cited references. Accordingly, Applicant traverses the above rejections and requests reconsideration.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In the present case, Applicant submits the prior art does not teach or suggest all of the limitations of at least the independent claims. For example, claim 10 recites a microprocessor:

> "receiving first interrupts from an interrupt controller, the first interrupts having architecturally fixed interrupt priorities, the microprocessor comprising:
>
> a core, for executing instructions, said core generating second interrupts;
>
> priority storage logic coupled to said core, for storing programmable priorities for said second interrupts; and
>
> a priority encoder, coupled to said core, and to said priority storage logic, for receiving the first and said second interrupts, and for prioritizing the first and said second interrupts utilizing the architecturally fixed interrupt priorities for the first interrupts, and said programmable priorities stored in said priority storage logic for said second interrupts."

In paragraph 8 of the present Office Action, the examiner states:

> "In reference to Claim 10, MCF5206 discloses a microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the first interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5), the microprocessor comprising: a core for executing instructions (See Page 1 Paragraph 3); and generating second interrupts by devices internal to the microprocessor (See 'Interrupt Controller' on Page 5). Because the interrupt priorities are programmable, MCF5206 will inherently include priority storage logic for storing the programmable priorities of the second interrupts (See 'Interrupt Controller' on Page 5)." (emphasis added).

However, claim 10 recites that the second interrupts are core generated interrupts and the priority storage logic is for storing programmable priorities for the core generated interrupts. In contrast, MCF5206 discloses an interrupt controller which provides user-programmable control of only non-core generated interrupts (the 3 or 7 external interrupts and the 5 internal peripheral interrupts). Additionally, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Therefore, MCF5206 does not inherently include priority storage logic for storing the programmable priorities of (core generated) second interrupts as suggested. At best, MCG5206 may suggest priority storage logic for storing programmable priorities of non-core generated interrupts.

In addition, the examiner states with respect to claim 10:

> "MCF5206 does not disclose that the second interrupts are generated by the core. Watanabe teaches a CPU core comprising segments commonly used to form a complete microprocessor, such as timers and I10 units (See Column 1 Lines 55-57 and Column 2 Lines 50-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the MCF5206 with the internal peripheral devices as part of the core . . . in order to allow it to be easily interfaced with various peripheral devices, to minimize the area needed by the microprocessor by reducing the area needed for connecting lines, and to provide greater flexibility in program design (See Column 1 Lines 42-45; Column 3 Lines 41 -46; and Column 4 Lines 1-16 of Watanabe)."

However, Applicant submits the combination does not produce the claimed invention as suggested. Further, as discussed below, Applicant submits one would not have been motivated to modify the MCF5206 processor as suggested. Applicant has reviewed both MCF5206 and Watanabe and neither MCF5206 nor Watanabe disclose programmable priorities for core generated interrupts or "priority storage logic coupled to said core, for storing programmable priorities for said second interrupts." Watanabe teaches nothing concerning the generation of interrupts, priorities of interrupts, programmable priorities, or anything else concerning interrupts. In fact, the word interrupt only occurs once in Watanabe where it says a processor may include an interrupt control register. As discussed above, MCF5206 only discloses programmable control of non-core generated interrupts. Therefore, even if one could show that combining MCF5206 and Watanabe would result in core generated interrupts, it does not necessarily follow, and is not inherent, that the core generated interrupts may be programmably controlled. In fact, Applicant's description clearly describes prior art wherein that is not the case. Consequently, Applicant submits the combination of cited art does not produce the invention as presently claimed in claim 10.

Applicant further submits a proper motivation to combine MCF5206 and Watanabe has not be proffered. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also

suggests the desirability of the combination. In the present Office Action, the Examiner states regarding claim 10 that:

> "it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the MCF5206 with the internal peripheral devices as part of the core . . . in order to allow it to be easily interfaced with various peripheral devices, to minimize the area needed by the microprocessor by reducing the area needed for connecting lines, and to provide greater flexibility in program design (See Column 1 Lines 42-45; Column 3 Lines 41 -46; and Column 4 Lines 1-16 of Watanabe)."

As can be seen from the above, a variety of reasons for making such a combination are offered. However, Applicant disagrees with the suggested reasons and submits one would not have been motivated to make the modification(s) suggested. Additionally, Applicant submits the proposed modifications would render the MCF5206 unsatisfactory for its intended purpose. MPEP 2143.01 states "if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

Moore's Law dictates that transistor density doubles every two years, and thus the design complexity of integrated circuit (IC) designs may increase significantly. Accordingly, design methodologies change over time to track the IC design complexity. The filing date for Watanabe occurred over a decade before the MCF5206 integrated microprocessor was constructed, and over 15 years earlier than the filing date of the present application. Column 2, lines 44-55, of Watanabe discloses a CPU core which comprises 3 internal peripheral devices such as a timer, a serial I/O, and an address register. In contrast, MCF5206 at pages 1-2, 4-5 and in Figure 1 teaches a much more complex integrated microprocessor with 8 internal peripheral devices that each may contain multiple components within (e.g., "timer module includes 2 general-purpose timers ... for use in any of 3 modes."). Figure 2 and column 3, lines 10-32, of Watanabe teaches that the function blocks have the same byte-size and block size, or should be configured as same block sizes, which leads to "the area needed for the function blocks is minimized." In MCF5206 the internal peripheral devices contain numerous different

byte-sizes as shown in the figure on page 6 and the descriptions on pages 4-5. Figure 2 of Watanabe discloses a CPU with far fewer buses than the MCF5206 integrated microprocessor, which is shown in both Figure 1 and in the figure on page 6. Watanabe has buses of fixed size, whereas the MCF5206 integrated microprocessor does not. Watanabe nowhere discloses pipeline registers, prefetching of instructions, or a dual-ported register file as does the more complex MCF5206 processor. As disclosed on page 3 of MCF5206, the core of the MCF5206 integrated microprocessor "consists of two independent, decoupled pipeline structures" that prefetch instructions and includes a dual-ported register file. Thus, one of ordinary skill in the art would conclude that the prior art of MCF5206 cannot be modified according to the floorplanning of Watanabe without significant increases in cost and complexity.

Additionally, the Examiner states a reason for the proposed modification is "to allow it to be easily interfaced with various peripheral devices". However, while such a modification may alter the interface between the MCF5206 core and the internal peripheral devices, it does not alter the external interface between the microprocessor and the peripheral devices. As noted on page 1 of MCF5206, the processor already includes common system functions on a chip and provides glueless interfaces. Thus, such a modification of the MCF5206 would not allow it to be more easily interfaced with various peripheral devices.

The Examiner states another reason for the proposed modification is "to minimize area needed by the microprocessor by reducing the area needed for connecting lines". For all the differences listed above between Watanabe and MCF5206, the floorplanning strategy of Watanabe to reduce the area for connecting lines is not applicable to the very different processor of MCF5206. Also the proposed modification may in fact *increase* the number of lines being routed as the internal peripheral devices would now be connected directly to the core components versus having the system bus controller handling the interface.

The final reason the Examiner gives for the proposed modification is "to provide greater flexibility in program design". However, all of the software operations listed at column 1, lines 3-10, of Watanabe are listed in the ISA in MCF5206 Addendum. Consequently, this suggested motivation is not present either.

For the reasons above the Applicant respectfully suggests that claim 10 is not anticipated by MCF5206, taken alone or in combination with Watanabe. Therefore, independent claim 10 is believed patentably distinct from the cited art. Each of claims 1 and 27 are patentably distinct for at least reasons similar to those given above.

In addition to the reasons given above, Applicant submits claim 27 is patentably distinct for further reasons. Claim 27 recites:

> "A method for prioritizing core generated interrupts and off-core interrupts within a processing system, comprising:
>
> receiving the off-core interrupts, the off-core interrupts having architecturally fixed interrupt priorities;
>
> receiving the core generated interrupts, the core generated interrupts having programmable priority levels which are intermediate to the architecturally fixed interrupt priorities for the off-core interrupts; (emphasis added)
>
> sorting the received off-core and core generated interrupts according to their priority levels; and
>
> producing an indication of which of the received off-core and core generated interrupts has the highest priority." (emphasis added)

Applicant has reviewed the MCF5206 reference and submits that MCF5206 does not disclose or suggest "the core generated interrupts having programmable priority levels which are intermediate to the architecturally fixed interrupt priorities for the off-core interrupts". Rather, page 5 of MCF5206 includes nothing more than a brief statement that the interrupt controller may provide up to seven interrupts for each of the external and internal interrupts and any one of four priority levels. However, it does not

disclose the priorities for on-core and off-core interrupts are intermediate of one another. MCF5206 describes the three external interrupts may be configured as fixed interrupt levels 1, 4 and 7 – each being programmed to one of four priority levels. However, there is no suggestion that the second interrupt priorities are intermediate to the fixed interrupt priorities. Further, Watanabe merely states that a microprocessor may comprise an interrupt control register (column 1 lines 16-22). However, Watanabe does not disclose anything concerning interrupt priorities, much less concerning interrupt priorities being intermediate of one another. Accordingly, Applicant submits claim 27 is patentably distinct from the cited art, taken either singly or in combination, for at least these additional reasons.

For all of the foregoing reasons, Applicant submits the pending claims are patentably distinguishable from the combination of cited art and a prima facie case of obviousness has not been established. Should the examiner believe reasons remain which would prevent the present application from proceeding to allowance, the below signed representative requests a telephone interview to facilitate a resolution and/or otherwise clarify any remaining issues for purposes of further prosecution or appeal.

CONCLUSION

Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested.

Also enclosed herewith are the following items:

☒ Petition for Extension of Time

Respectfully submitted,

/James W. Huffman/

Reg. No. 35,549
ATTORNEY FOR APPLICANT(S)